COURSE NUMBER & TITLE: ELTR 2610, 01 - Advanced Microprocessors

SEMESTER/YEAR: Fall 2006

LECTURE HOURS: 3  LAB HOURS: 3  CREDIT HOURS: 4.5

CLASS TIME: Lecture: 11-11:50 a.m.  MWF  ROOM: EI 124
Lab: 1-3:50 p.m.  M  EI 124

INSTRUCTOR’S NAME: Jonathan Blesi

INSTRUCTOR’S CONTACT INFORMATION:
Office Location: EI 118
Office Phone: 268-2459
Email: jblesi@caspercollege.edu

OFFICE HOURS: MWF 10:00-10:50 am
W 1:00 -1:50 pm
TH 12-12:50 pm (CS 140)

COURSE DESCRIPTION: Application of 16 and 32 Bit INTEL microprocessors to selected problems of data handling, graphics, and personal use. Program debugging and assembler/compiler languages.

STATEMENT OF PREREQUISITES: ELTR 1770, or permission of the instructor.

GOAL: The student will:

1. Write assembler language programs in both 16 and 32 bit INTEL assembler language to interface with both memory and peripheral subsystems.

2. Make use of student subroutines, BIOS calls and DOS based functions to achieve this interface.

3. Identify the functions of all chip subsystems on motherboards built with the above microprocessors.

OUTCOMES: Upon completion of this course, the student will:

1. Understand the architecture of the 80286, 80386, 80486 and Pentium INTEL CPU’s and how they are interfaced with peripheral devices.

2. Understand system memory architectures in 16, 32 and 64 bit data bus systems built with the above CPU’s.

3. Understand how cache memory works in high performance systems based on the above microprocessors.

METHODOLOGY: See Attachment
EVALUATION CRITERIA: ELECTRONICS 2610 GRADING GUIDELINES

Full tests - total of four, each worth 100 points 400 pts
Lab reports - total of eight, six 10 pts, two 20 pts 100 pts
Grand Total 500 pts

Semester average = Grand total / 500

Letter Grade Semester Average
A 90.0-100.0
B 80.0-89.9
C 70.0-79.9
D 60.0-69.9
F 0.0-59.9

REQUIRED TEXT, READINGS, AND MATERIALS:
The Advanced INTEL microprocessors - Architecture, Programming and Interfacing: Brey
8086 Micro reference card: Micrologic
Various handouts

CLASS POLICIES: Last date to change to Audit Status or to Withdraws with a W Grade: November 3, 2006.

SAFETY: Personal and equipment safety standards will be strictly enforced. It is the individual’s responsibility to develop a safe work attitude.

STUDENT RIGHTS AND RESPONSIBILITIES: Please refer to the Casper College Student Conduct and Judicial Code for information concerning your rights and responsibilities as a Casper College Student.

Chain of Command: If you have any problems with this class, you should first contact the instructor in order to solve the problem. If you are not satisfied with the solution offered by the instructor, you should then take your problem through the appropriate chain of command starting with the department head, then the division chair, and lastly the vice president for academic affairs.

Academic Dishonesty- Cheating and Plagiarism: Casper College demands intellectual honesty. Proven plagiarism or any form of dishonesty associated with the academic process can result in the offender failing the course in which the offence was committed or expulsion from school. See the Casper College Student Code of Conduct.

ADA Accommodations Policy: It is the policy of Casper College to provide appropriate accommodations to any student with a documented disability. If you have a need for accommodation in this course, please make an appointment to see me at your earliest convenience.
CALENDAR OR SCHEDULE INDICATING COURSE CONTENT:

Unit-1 Introduction to the 80286
   The evolution of the 16 bit microprocessor
   Basic 80286 Architecture
   Memory model 80286, 80386, 80486
   The programming model
   Data formats

Unit-2 Addressing Modes
   Register addressing
   Immediate Addressing
   Direct Addressing
   Register indirect addressing
   Indexed addressing
   Stack addressing

Unit-3 Simple Data Movement & Arithmetic Instructions
   MOV revisited
   Addition and subtraction
   Simple shifting
   Basic logic instructions

Unit-4 Advanced Arithmetic & Logic Instructions
   Multiplication and division
   Rotation and shifting
   BCD and ASCII arithmetic
   The jump group
   String instructions
   Subroutines, CALL and RET

Unit-5 80286 Hardware Specifications
   Pinouts and pin functions
   82284 clock generator
   Bus buffering and latching
   A minimum mode system
   82288 bus controller
   A maximum mode system

Unit-6 Memory Interface
   80286 memory interface
   A typical array of EPROM
   A typical array of Static RAM
   Interfacing Dynamic RAM

Unit-7 Peripheral Chips Needed for a Complete System
   8253, 8254 counter timer
   8259 INT controller in brief
   8237 DMA controller
   8251 USART
Unit-8 I/O Interface
   Basic I/O interface
   Simple I/O ports
   8255 PPI

Unit-9 Interrupts
   Basic interrupt processing
   Software interrupts
   Hardware interrupts
   8259 interrupt controller

Unit-10 8087 Family of Math Coprocessors
   808x7 architecture
   Data formats
   80287 instruction set

Unit-11 Introduction to the 80386
   80386 architecture
   80386 32 bit register set
   An introduction to 32 bit 80386 programming
   80386DX / 80386SX pinouts and differences
   80386 addressing modes pipelined and nonpipelined
   Memory timing for pipelined addressing
   Interleaved memory

Unit-12 80386 Bus Interfaces
   80386 bus interface and bus control
   32 bit memory bus interface
   An introduction to cache memory
   82385 cache controller chip

Unit-13 80486 Advanced 32 Bit CPU
   Introduction to 80486
   Advanced 80486 features

Unit-14 The Pentium, a Superscalar 32 Bit CPU
   Introduction to Pentium/80586
   Advanced Pentium features
   Pentium II
   Celeron
   Pentium III
   Pentium 4